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Asymmetrical Contact Geometry to Reduce Forward-Bias Degradation in β-Ga_2O_3 Rectifiers

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We report a study of the effect of different Schottky contact orientations on maximum current achievable before failure and also temperature distributions in vertical geometry Ga_2O_3 rectifiers. Due to the strong anisotropy of thermal conductivity in Ga_2O_3, asymmetrical Schottky contacts are needed to provide higher current density with enhanced lateral thermal dissipation, symmetrical temperature profile and lower junction temperature at a specific diode current density compared to symmetrical contacts. Devices with rectangular contacts fabricated on (001) orientated wafers with their long axis perpendicular to the [010] crystallographic direction show much greater resistance to thermal degradation under forward bias conditions than either square contact rectifiers or those oriented with their long axis oriented perpendicular to the [100] direction. An optimized contact orientation can produce a 25% increase in maximum forward current. Practical operating conditions for Ga_2O_3 power devices will need to encompass all aspects of thermal management, including these geometric factors as well as active and passive cooling.
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Power electronics are responsible for controlling and converting electrical power to provide optimal conditions for transmission, distribution, and load-side consumption.[1–3] This is becoming increasingly important, as renewable energy sources such as solar and wind power need to be switched into the existing power grid and electric vehicles need dc-to-ac converters and charging infrastructure. Since a significant portion of electricity is controlled through power electronics, more efficient power converters offer substantial energy savings. Specific applications for semiconductor power conversion and control electronics include transportation electrification (ground, marine, and air), renewable energy generation, energy storage, grid modernization (solid-state transformers and DC distribution), and electronic loads (light-emitting diode lighting and data centers).[2,3] All of these applications demand power electronics to be more efficient, smaller, more reliable and less expensive.

Si devices have disadvantages relative to wide bandgap semiconductor devices in terms of higher on-state resistance, with concurrent higher conduction losses, limited temperature range of operation and low switching frequencies.[3] Higher efficiencies can be obtained with wide bandgap semiconductors. Higher critical electric fields in these materials enable thinner, more highly doped voltage-blocking layers, which can reduce on-resistance by up to two orders of magnitude in majority carrier devices compared to Si. The two most developed wide bandgap semiconductors are SiC[4–8] and GaN,[9–15] with SiC now commercialized for many applications in power management and GaN being used in X-/Ku-band RF power devices and monolithic microwave integrated circuits (MMICs). Even higher power figures-of-merit are theoretically possible with BN, diamond, high-Al AlGaN and Ga_2O_3.[16–23] The latter is particularly attractive because of the economics of its bulk crystal growth, which should reduce the cost of the technology relative to the other ultra-wide bandgap semiconductors.[24,25]

However, although it is a promising candidate for the high-power electronics used in inverter and power low control systems, Ga_2O_3 suffers from a low thermal conductivity relative to GaN and SiC.[26–29] Moreover, the thermal conductivity is strongly anisotropic, with values at room temperature ranging from 27 W m-K^{-1} in the [010] crystallographic direction to only 11 W m-K^{-1} in the [110] direction, as shown in Fig. 1. These thermal conductivities are more than an order of magnitude lower than the values for GaN (210 W m-k^{-1}) and SiC (270 W m-k^{-1}). The anisotropy mainly originates from anisotropic phonon dispersion. The other disadvantage is that the thermal conductivity falls rapidly with temperature, so that high temperature device operation is particularly problematic with Ga_2O_3.[30–34] It is expected that thermal energy will need to be efficiently extracted from interfacial thermal contacts to Ga_2O_3 into high-thermal-conductivity substrates, or through the electrical contacts on the devices. Specialized high-performance methods for thermal management in microelectronics, including microchannel heat sinks and micropumps, jet impingement, flat heat pipes, and phase-change solid and fluid media for energy storage and contact conductance.[35–40] Other approaches include integrated liquid microchannel cooling systems such as direct die-attach microconvective cooling via high velocity fluid jets, microscale ion-driven air flow, and piezoelectric coolers.[37–40] Microchannel heat sinks and micropumps provide very high heat transfer coefficients. Microchannel heat sinks are compact, making them compatible for thermal management of electronics.

A potential early insertion point for Ga_2O_3 devices is for vertical geometry Schottky rectifiers, based on the availability of both thick epitaxial layers and conducting substrates.[30–33] To achieve high reverse blocking capability in Ga_2O_3 rectifiers, a low doped n-type epitaxial layer is required, which leads to lower electrical conductance and in turn exacerbates heat generation in the epitaxial layer. Under deliberately induced failure at high current forward bias conditions, cracks may appear on the Schottky contact and delamination along the [010] crystal orientation has been observed.[31,32] The failure mechanism has been mainly ascribed to plastic deformation of the lattice structure during device self-heating. Previous thermal simulations have shown that the main mechanism of heat generation in a vertical β-Ga_2O_3 Schottky device is Joule heating, and the highest temperature was observed near the metal-epi interface.[34] Therefore, optimized thermal management has become a key consideration for advancement

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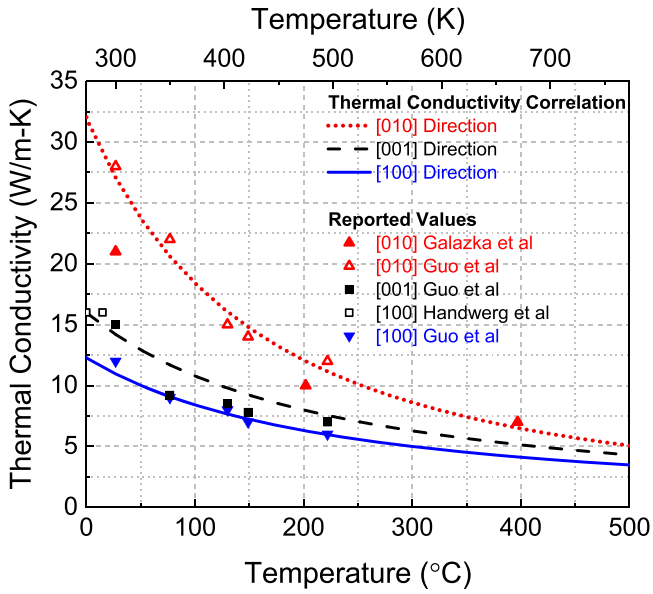

Figure 1. Temperature dependence of the thermal conductivity of β-Ga_2O_3 in different crystallographic directions.

in device performance and mitigation of potential device failure under high-power operation conditions.[1]

We have previously shown that over a broad range of Schottky contact size (40–800 μm diameter), the devices fail at similar temperatures (270 °C–350 °C), independent of area, but that the current density at which failure occurs under forward bias is a strong function of contact size.[31] For example, small devices (40 μm diameter) were able to achieve a forward current density of $\sim$2200 A.cm^{-2} before failure, while large devices (800 μm diameter) failed at $<$ 200 A.cm^2. The anisotropic thermal conductivity suggests that contact orientation may also play a role in determining the forward bias failure conditions.[31]

In this paper, we report on the orientation dependence of the Schottky contact on Ga_2O_3 rectifiers on the maximum achievable forward currents and the forward voltage threshold for the onset of thermally-induced damage. The use of asymmetric Schottky contacts with their long axis perpendicular to the [010] crystallographic direction is the optimum choice to maximize forward currents. This is a part of an effort to better understand thermal gradients in rectifiers to better understand device performance and to link these to fundamental failure and reliability mechanisms.

Experimental

The fabrication sequence for the Schottky rectifiers has been described previously,[30–33] but in brief, begins with a layer structure of 10 μm Si-doped (3.5 $\times$ 10^{16} cm^{-3}) epitaxial layer grown by Halide Vapor Epitaxy (HVPE) on (001) orientated 650 μm β-phase Sn-doped (n = 3.6 $\times$ 10^{18} cm^{-3}) Ga_2O_3 substrate (Novel Crystal Technology). A full area backside Ohmic contact (20 nm/80 nm Ti/Au) was deposited by electron beam (e-beam) evaporation and annealed for 30 s at 550 °C in N_2 using an SSI SOLARIS 150 rapid thermal annealer. To form a field plate, 40 nm Al_2O_3 and 360 nm SiN_x dielectric were deposited using Cambridge-Nano-Fiji Atomic Layer Deposition and Plasma-Therm Plasma Enhanced Chemical Vapor Deposition tools, respectively. Windows with different geometries (0.25 $\times$ 0.5 mm^2 rectangles with the long axis oriented perpendicular to either the [100] or [010] crystallographic directions or 0.354 $\times$ 0.354 mm^2 squares of the same area) were opened using 1:10 diluted Buffered Oxide Etchant (BOE). Figure 2 shows images of the different contact orientations and shapes. The purpose of having these different Schottky contact geometries was to test the orientation dependence of forward bias current and resistance to damage under forward biasing stressing. The sample surface was then treated in O_3 for 20 min to remove hydrocarbon and other contamination species. 400 μm Ni/Au (80 nm/320 nm) Schottky metal was subsequently deposited using E-beam evaporation with standard acetone lift-off.

The rectifier forward and reverse current-voltage (I-V) characteristics were recorded on a Tektronix 370-A curve tracer. For forward bias stressing of the rectifiers, an Agilent Technologies 8114A pulse generator was used to apply continuous voltage bias at 95% duty cycle for 1 min at various voltage levels up to the point of device failure. The forward voltage was increased gradually by 1 V until a sudden irreversible increase of the reverse bias leakage current and irreversible decrease of breakdown occurred at a given reverse bias voltage. The forward currents were corrected for the probe resistance of 1.34Ω. Thermal images of the sample were taken using an Optris PI640 infrared camera. Some in situ Transmission Electron Microscopy images of devices operated to the failure point were taken using electron transparent functional specimens from the fabricated bulk β-Ga_2O_3 Schottky diode using focused ion beam (FIB).[41–43] Electrical characterization was performed inside a field emission 200 kV FEI Talos F200X TEM equipped with energy dispersive spectroscopy (EDS) with 1.2 Å resolution.

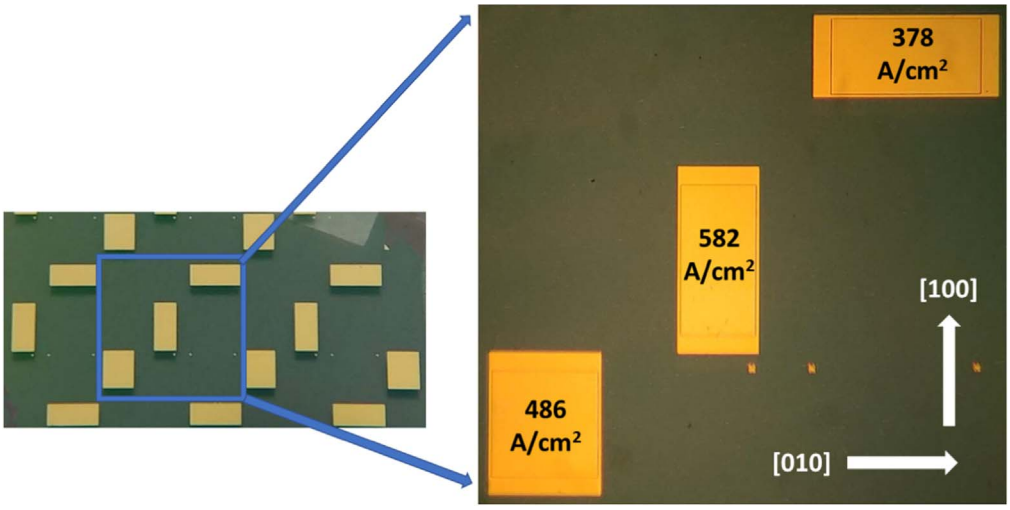

Figure 2. Optical microscope images of 0.25 $\times$ 0.5 mm^2 rectangular Schottky rectifiers oriented with their long axis perpendicular to either [100] or [010] orientations and a standard square geometry rectifier of the same area. The maximum current density achievable with each orientation is also shown.

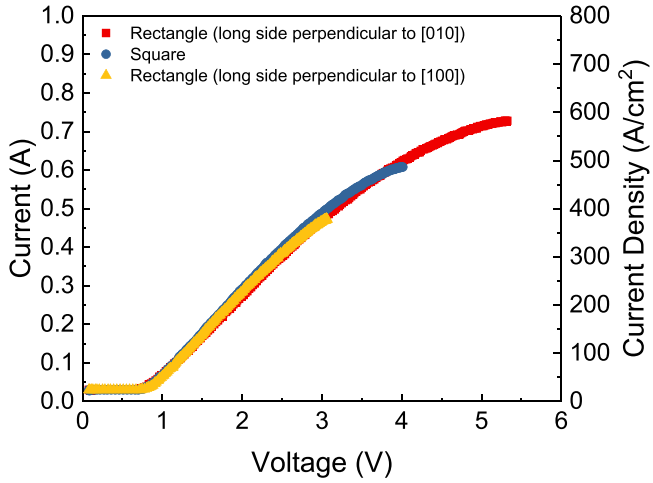

Figure 3. Forward I-V characteristics from the rectangular rectifiers oriented in the two different crystallographic directions and also the control (square) rectifier of the same area.

For thermal simulations, a 3-D finite element analysis was employed to calculate the temperature distribution. The details of this steady state energy balance approach have been given previously. The steady state temperature contours of the rectifiers with various geometries were simulated at the maximum forward bias measured experimentally. The highest junction temperature at the center of the metal contact was used to compare the temperature rises of the different contact geometries and orientations.

Results and Discussion

Figure 3 shows forward I-V characteristics up to the failure point for rectifiers with either rectangular shaped contacts oriented in the two different directions, or the square contacts. Note that the absolute forward currents reached range from 0.48 A to 0.74 A, corresponding to current densities of 384–592 A cm^{-2} current density. Orienting the rectangular shaped contacts with the long side perpendicular to the [010] crystallographic direction in the Ga_2O_3 produces the largest current by ~0.14 A relative to the square shape, while placing the long side perpendicular to [100] produces a similar penalty of 0.13 A relative to the square control contact. This is a clear demonstration of the need to take account of the anisotropic thermal properties of Ga_2O_3.

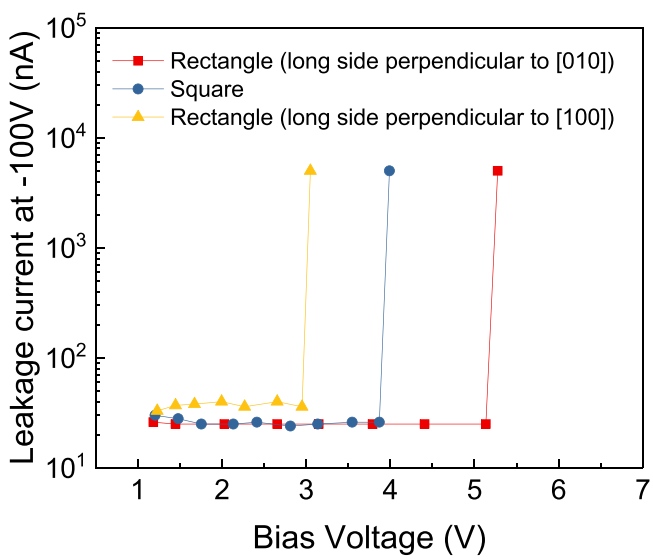

Figure 4. Reverse leakage current at −100V reverse bias for the different oriented rectangular rectifiers and the square rectifier, as a function of the forward bias at failure.

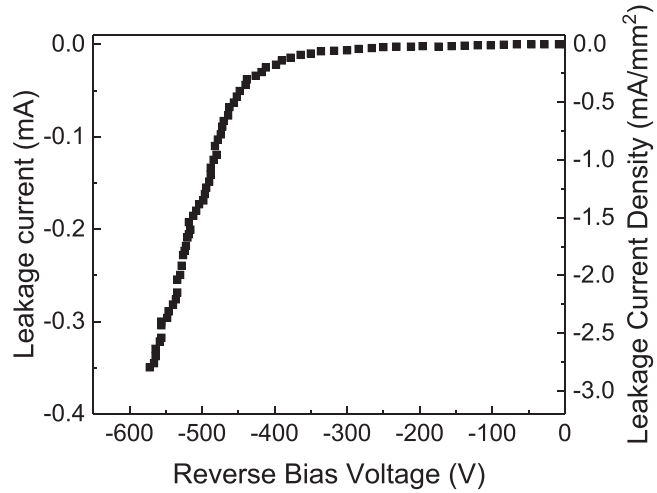

Figure 5. Device leakage current and current density as a function of reverse voltage bias.

Figure 4 shows the leakage current at −100V reverse bias for the three different geometry rectifiers as a function of the forward bias to which the devices were subjected. The three devices show a clear difference in the forward bias at which the onset of degradation, as measured by the sudden and concurrent increase in reverse current, is observed. The use of asymmetric Schottky contacts oriented in the correct direction can increase the threshold at which device degradation occurs by taking advantage of the higher thermal conductivity in the [010] direction. Figure 5 shows the full spectrum of device reverse leakage current vs voltage bias, where the device breakdown was defined as 3 mA cm^{-2}. A breakdown voltage of ~570 V was reported in this work, which is consistent with previously reported 10 μm epi device.

The rectifiers that failed consistently showed delamination of the epitaxial layer. There were also multiple crack lines observed along the [010] direction. Figure 6 shows a scanning electron microscope (SEM) image of a after forward biasing to failure. Note the oriented cracks that appear on the epitaxial layer surface-these eventually lead to complete delamination of this layer along the [101]

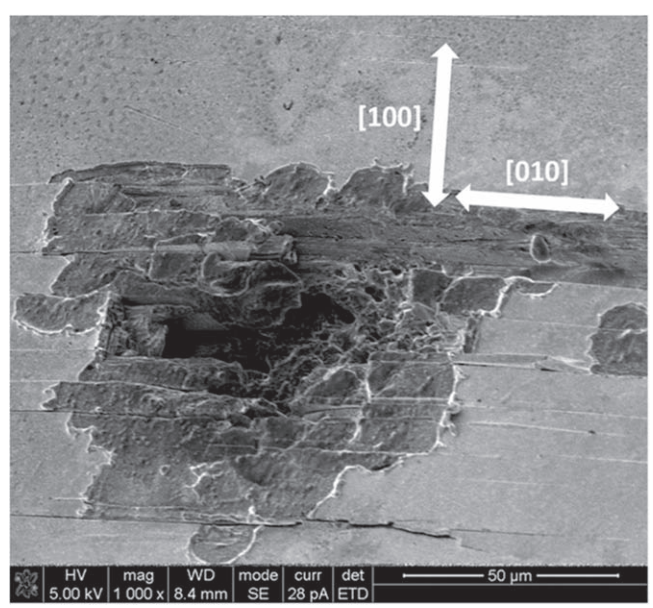

Figure 6. SEM micrograph of rectifier after forward biasing to failure.

crystallographic direction.[31,32] Previous ultra-fast laser irradiation experiments[44] showed that the inability to dissipate the heat in Ga_2O_3 produces mechanical failure of the material along natural cleavage planes. The concentration of heat in the lightly doped epitaxial layer relative to the heavily doped substrate leads to differential thermal expansion and delamination of the epitaxial layer. Raman mapping of Ga_2O_3 Schottky rectifiers confirms the concentrated heat generation near the metal/Ga_2O_3 interface.[45] We have observed this for many samples, from different wafers and different contact sizes and orientations.

The in situ TEM was also instructive. Figure 7 shows I-V's and TEM cross-sectional images of the symmetric contact rectifiers before and after failure. These rectifiers were formed into a TEM coupon by focused ion beam milling and thus one cannot compare the I-V's to the thin film devices. The current densities are shown on both log and linear scales at the top left and bottom right corner of the figure to amplify the differences, while TEM bright field images are shown for the total forward current through the electron transparent foil. There are defect clusters created near the top and bottom electrodes, which occur prior to the cracking and delamination. The elemental compositions in these clusters derived from the EDS data is shown in Fig. 8. There is a gold (Au) ball formed on the top surface as the cathode degrades, as well as Ga-rich and Au-Si-rich droplets formed within the Si-doped Ga_2O_3 epitaxial layer. These are stable to the point where the cracking and delamination leads to complete failure of the device. It will be interesting to see if the asymmetric contact design delays the creation of these droplets relative to the symmetric contact design.

Figure 9 shows the steady state thermal simulation temperature profiles on the epi surface for the three different contact geometries, with the rectifiers biased at the corresponding failure condition. The anisotropic thermal conductivity leads to oval-shaped temperature patterns adjacent to the contact the thermal pictures for all three geometries, but a lower maximum temperature for the rectangular contact oriented perpendicular to [010]. The simulations assumed constant current density over the entire contact area, but the spreading resistance on the metal contact could lead to current crowding during experimental measurements with a probe.[31] The experimental profiles recorded on the thermal camera under different contrast conditions are shown in Fig. 10. These were obtained at a current density of $\sim$120 A cm^{-2}. We observe a circular temperature profile for the optimized oriented rectangular contact, oval for the square device, and a strong oval pattern for the rectangular device oriented with the long side perpendicular to [100]. For diodes with the same surface but only with different orientation, it is clear that the [100] direction greatly facilitate the dissipation of heat and enables a more spread-out thermal profile for diode with long edge perpendicular to this direction, and therefore a higher surface area for lateral thermal dissipation through the bottom heat sink. The impact of the anisotropic thermal conductivity is very pronounced in terms of the temperature profile generated.

Figure 11 shows the current performance for the state-of-the-art Ga_2O_3 vertical Schottky diodes in terms of breakdown voltage vs the maximum measured current Fig. 11a and current density Fig. 11b. A strong negative correlation can be found between the diode current and their respective breakdown voltage. The optimized diode design is inline with the published datapoints, and with the improvement of material growth, the breakdown voltage is expected to continue to improve for larger sized diode.[17,30–33,46–58]

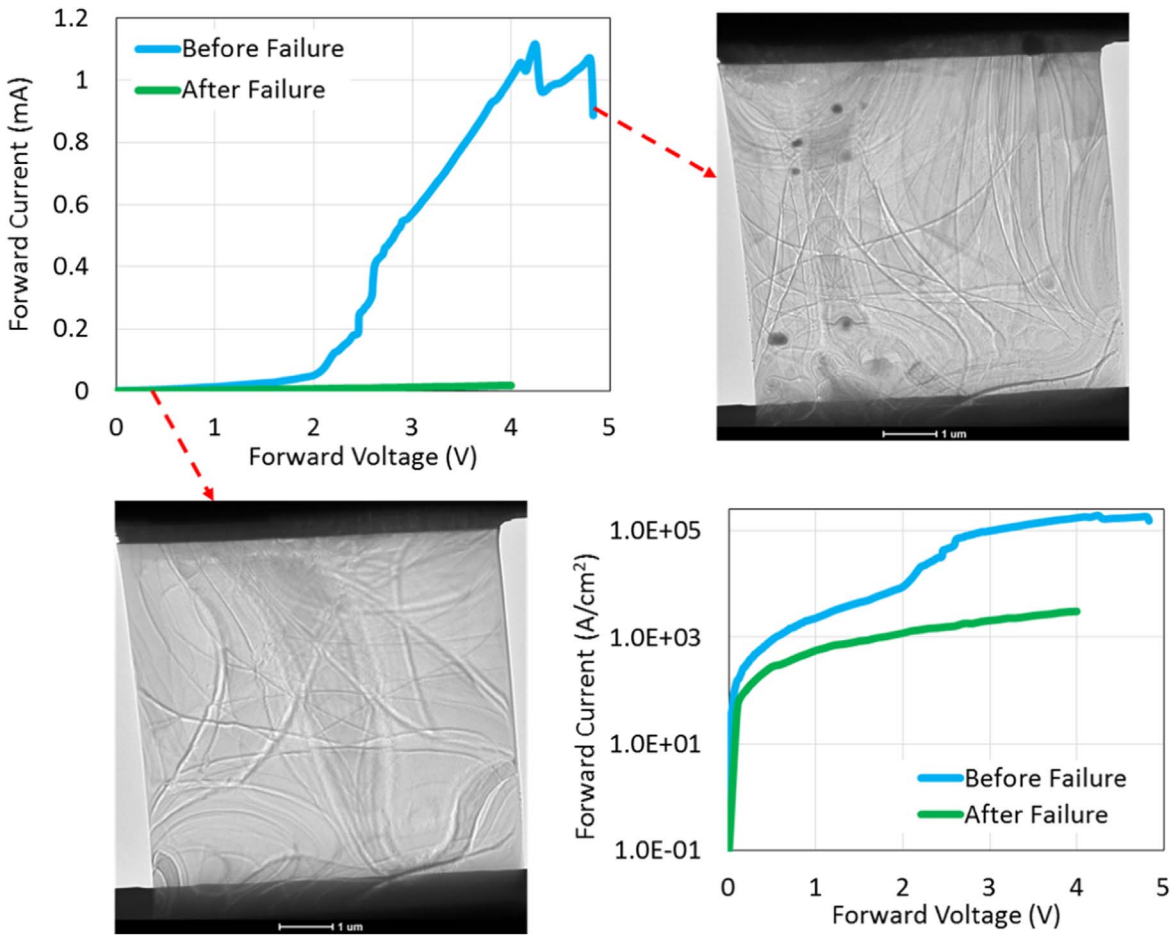

Figure 7. In situ TEM micrographs of rectifiers before and after failure under forward bias conditions. The corresponding I-Vs and current densities are also shown for each condition.

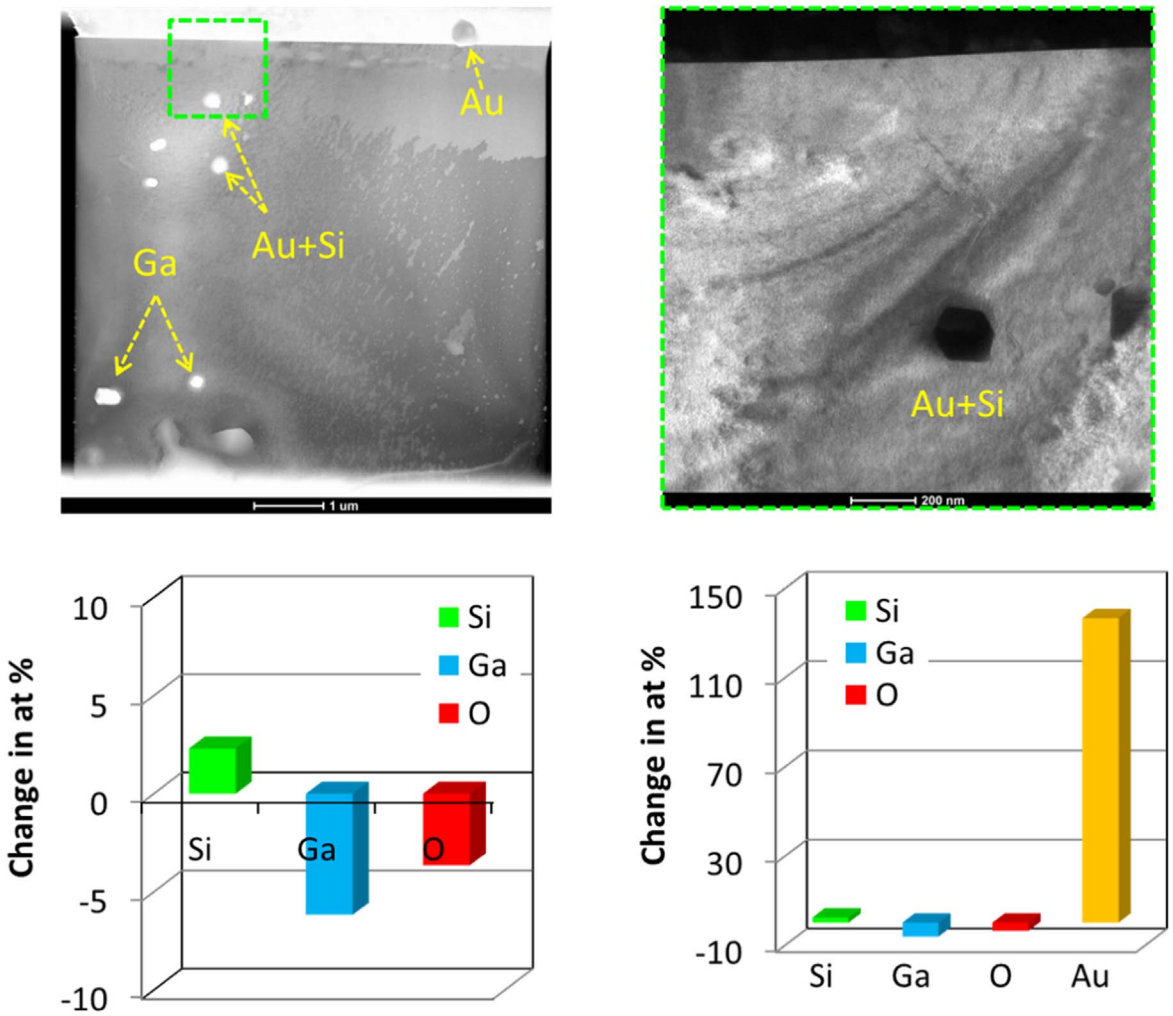

Figure 8. TEM and EDS data to identify the chemical composition in the observed defect clusters produced in the symmetric contact rectifiers by forward biasing. The Schottky contact is at the top of each image, while the bottom is the Ohmic contact.

Conclusions

The current state-of-the-art β-Ga_2O_3 vertical Schottky rectifiers are now reaching forward currents where thermal-induced failure can occur due to plastic crystallographic deformation near the epi-substrate interface. The thermal interfaces between the epitaxial drift layer and the underlying substrate is a bottleneck for heat dissipation. With an Arrhenius relationship between device mean time to failure (MTTF) and operating temperature, small changes in the device temperature can result in orders of magnitude differences in lifetime.[38] The low and anisotropic thermal conductivity means that thermal management approaches are critical for Ga_2O_3. Direct evidence for this has been captured using an IR camera. One possible method that will form part of a larger scheme to address this is the fabrication of asymmetrical contacts along the higher thermal conductivity directions. It should be emphasized that in addition to device-level approaches, there is also a need for a holistic approach in which novel packaging materials, integration methods, and thermal management techniques that include transport across complex multi-material interfaces at the package and system levels are essential to produce Schottky rectifiers operating at realistic current

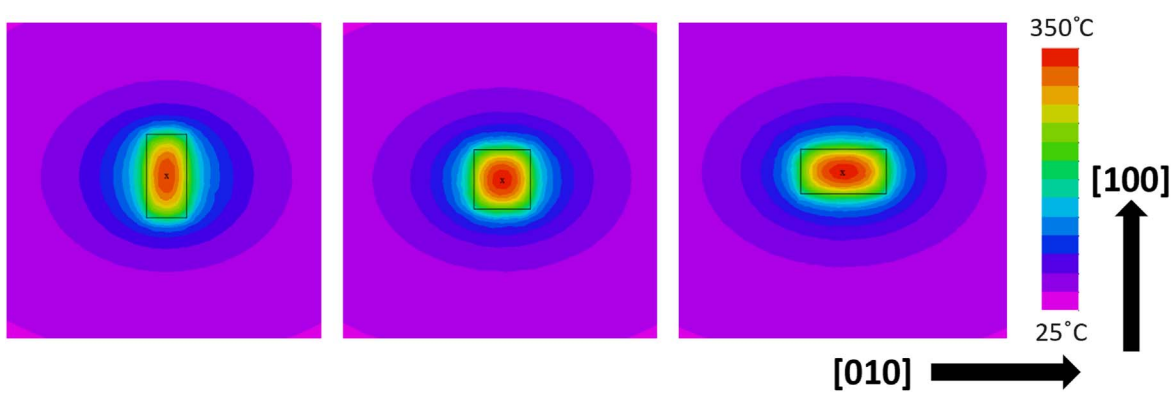

Figure 9. Simulated temperature distributions for different geometry rectifiers at their maximum forward bias.

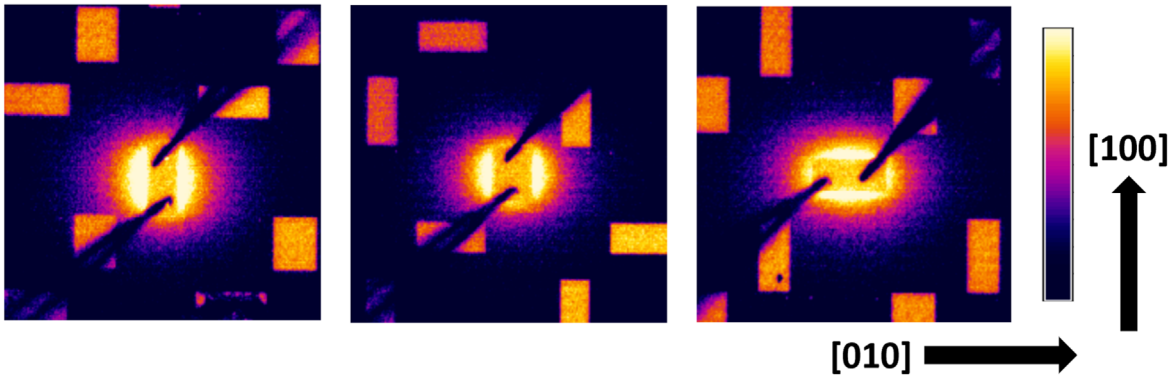

Figure 10. Thermal images of different geometry rectifiers at their maximum forward bias.

levels.[1,34–37,39,45,59] The traditional method of cooling electronic devices via heat spreading through thermal interface materials and high conductivity heat spreaders is likely insufficient for the applications envisaged for Ga_2O_3.[60]

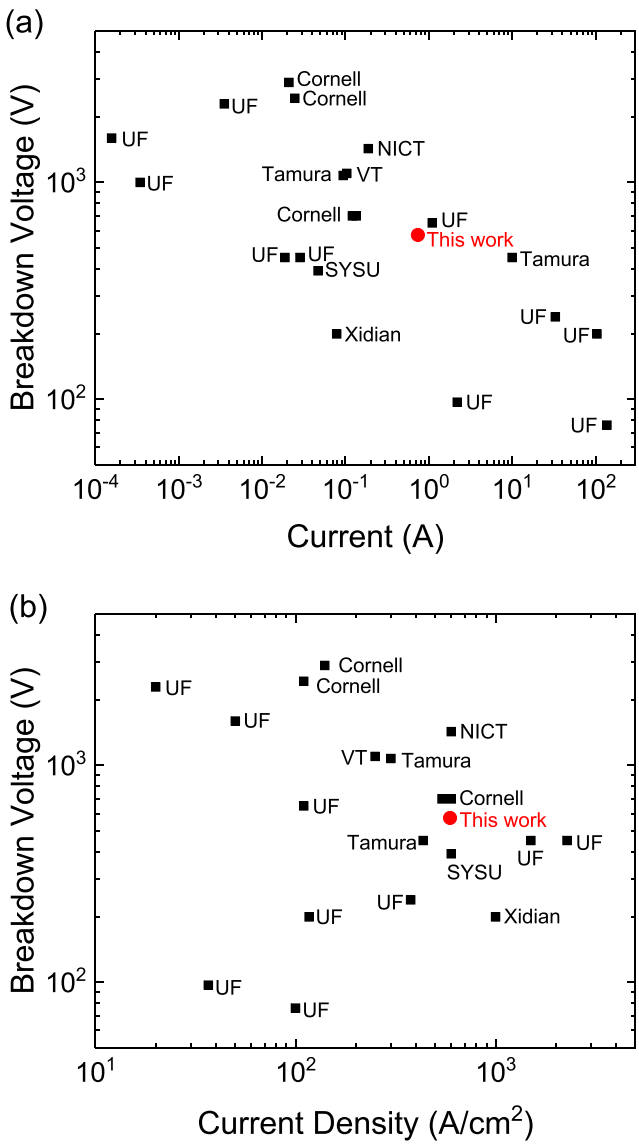

Figure 11. Comparison of diode breakdown voltage vs device maximum measured current (a) and current density (b).

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References

1. U.S. Department of Transportation, *Bureau of Transportation Statistics, Transportation Statistics Annual Report, Chap. 7* (2018).
2. D. Boroyevich, "CPES Research: SSPS—building blocks for the future electronic power grid, U.S. Department of energy solid-state power substation road mapping workshop." (North Charleston, SC) June 27 (2017).
3. "Basic research needs for microelectronics-report of the office of science workshop on basic research needs for microelectronics." October, 23 (2018).
4. K. Hamada, M. Nagao, M. Ajioka, and F. Kawai, *IEEE Trans Electron Dev.*, **62**, 278 (2015).
5. B. Whitaker, A. Barkley, Z. Cole, B. Passmore, D. Martin, T. R. McNutt, A. B. Lostetter, J. S. Lee, and K. Shiozaki, *IEEE Trans. Power Electron.*, **29**, 2606 (2014).
6. S. Banerjee, K. Matocha, K. Chatty, J. Nowak, B. Powell, D. Guttierrez, and C. Hundley, "Manufacturable and rugged 1.2 KV SiC MOSFETs fabricated in high-volume 150 mm CMOS fab." *Paper presented at 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, (Prague, Czech Republic) June (2016).
7. K. Matocha, S. Banerjee, and K. Chatty, *Mater. Sci. Forum*, **858**, 803 (2015).
8. E. Candan, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, *IEEE Trans. Power Electron.*, **31**, 3690 (2016).
9. Y. S. Noh, "A 16 Watt X-Band GaN high power amplifier MMIC for phased array applications." *IEEE International Conference on Microwave and Millimeter Wave Technology,* **Vol. 2**, p. 979 (2016).
10. A. Fong, *Electron. Lett*, **55**, 393 (2019).
11. R. Chen, *Electronics*, **8**, 27 (2019).
12. K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, *IEEE Electron Dev. Lett.*, **37**, 161 (2016).
13. O. Aktas and I. Kizilyalli, *IEEE Electron Dev. Lett.*, **36**, 890 (2015).
14. C. Gupta, C. Lund, S. Chan, A. Agarwal, J. Liu, Y. Enatsu, S. Keller, and U. Mishra, *IEEE Electron Dev. Lett.*, **38**, 353 (2017).
15. M. Sun, Y. Zhang, X. Gao, and T. Palacios, *IEEE Electron Dev. Lett.*, **38**, 509 (2017).
16. M. Higashiwaki, K. Sasaki1, H. Murakami, Y. Kumagai, A. Koukitu, A. Kuramata, T. Masui, and S. Yamakoshi, *Semicond. Sci. Technol.*, **31**, 034001 (2016).
17. K. Konishi, K. Goto, H. Murakami, Y. Kumagai, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, *Appl. Phys. Lett.*, **110**, 103506 (2017).
18. S. J. Pearton, J. Yang, P. H. Cary IV, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, *Appl. Phys. Rev.*, **5**, 011301 (2018).
19. M. A. Mastro, A. Kuramata, J. Calkins, J. Kim, F. Ren, and S. J. Pearton, *ECS J. Solid State Sci. Technol.*, **6**, 356 (2017).
20. T. P. Chow, I. Omura, M. Higashiwaki, H. Kawarada, and V. Pala, *IEEE Trans. Electron Dev*, **64**, 856 (2017).
21. S. J. Pearton, F. Ren, M. Tadjer, and J. Kim, *J. Appl. Phys.*, **124**, 220901 (2018).
22. Z. Hu, K. Nomoto, W. Li, N. Tanen, K. Sasaki, A. Kuramata, T. Nakamura, D. Jena, and H. G. Xing, *IEEE Electron Dev. Lett.*, **39**, 869 (2018).
23. Z. Hu et al., *Appl. Phys. Lett.*, **113**, 122103 (2018).

24. M. J. Tadjer, *The Electrochemical Society Interface*, **27**, 49 (2018).
25. S. B. Reese, T. Remo, J. Green, and A. Zakutayev, *Joule*, **3**, 903 (2019).
26. Z. Guo, A. Verma, X. Wu, F. Sun, A. Hickman, T. Masui, A. Kuramata, M. Higashiwaki, D. Jena, and T. Luo, *Appl. Phys. Lett.*, **106**, 111909 (2015).
27. M. Handwerg, R. Mitdank, Z. Galazka, and S. F. Fischer, *Semicond Sci. Techno*, **30**, 024006 (2015).
28. M. D. Santia, N. Tandon, and J. D. Albrecht, *Appl. Phys. Lett.*, **107**, 041907 (2015).
29. M. Slomski, N. Blumenschein, P. P. Paskov, J. F. Muth, and T. Paskova, *J. Appl. Phys.*, **121**, 235104 (2017).
30. J. Yang, F. Ren, S. J. Pearton, and A. Kuramata, *IEEE Trans. Electron Devices*, **65**, 2790 (2018).
31. M. Xian, R. Elhassani, C. Fares, F. Ren, M. Tadjer, and S. J. Pearton, *J. Vac. Sci. Technology B*, **37**, 061205 (2019).
32. J. Yang et al., *ECS J. Solid State Sci. Technol.*, **8**, Q3028 (2019).
33. F. R. Jiancheng Yang, S. J. Marko Tadjer, Pearton, and A. Kuramata, *ECS J. Solid State Sci. Technol.*, **7**, Q92 (2018).
34. E. Ribhu Sharma, M. E. Patrick, Law, F. Jiancheng Yang, Ren, and S. J. Pearton, *ECS J. Solid State Sci. Technol.*, **8**, Q3195 (2019).
35. S. Garimella, J. D. Killion, and J. W. Coleman, *J. Fluids Eng.*, **124**, 205 (2001).
36. D. G. Cahill, W. K. Ford, K. E. Goodson, G. D. Mahan, A. Majumdar, H. J. Maris, R. Merlin, and S. R. Phillpot, *J. Appl. Phys.*, **93**, 793 (2003).
37. A. Bartolini, R. Diversi, D. Cesarini, and F. Beneventi, *IEEE Design & Test*, **17**, 2168 (2017).
38. P. D. T. O'Connor, *Qual. Reliab. Eng. Int.*, **5**, 255 (1989).
39. K. M. Razeeb, Eric Dalton, G. L. William Cross, and A. J. Robinson, *Internat Mater Rev*, **63**, 1 (2018).
40. S. M. Walsh et al., *IEEE Trans Comp, Packaging Manuf Technol.*, **9**, 269 (2019).
41. Z. Islam, A. Haque, and N. Glavin, *Appl. Phys. Lett.*, **113**, 183102 (2018).
42. B. M. Wang, Z. Islam, A. Haque, K. Chabak, M. Snure, E. Heller, and N. Glavin, *Nanotechnology*, **29**, 31LT01 (2018).
43. Z. Islam, A. L. Paoletta, A. M. Monterrosa, J. D. Schuler, T. J. Rupert, K. Hattar, N. Glavin, and A. Haque, *Microelectronics Rel.*, **102**, 113493 (2019).
44. M. Ahn, A. Sarracino, A. Ansari, B. Torralva, S. Yalisove, and J. Phillips, *J. Appl. Phys.*, **125**, 223104 (2019).
45. B. Chatterjee, K. Zeng, C. D. Nordquist, U. Singisetti, and S. Choi, "Device-level thermal management of gallium oxide field-effect transistors." *IEEE Trans.Comp. Pack. Manu. Tech*, **9**, 2352 (2019).
46. J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, and A. Kuramata, *IEEE Electron Device Lett.*, **38**, 906 (2017).
47. W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, *IEEE Electron Device Lett.*, **41**, 107 (2020).
48. W. Li, Z. Hu, K. Nomoto, R. Jinno, Z. Zhang, T. Q. Tu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, *Tech. Dig. - Int. Electron Devices Meet.* (IEEE, NY, USA) p. 8–5–1 (2019).
49. C.-H. Lin et al., *IEEE Electron Device Lett.*, **40**, 1487 (2019).
50. N. Allen, M. Xiao, X. Yan, K. Sasaki, M. J. Tadjer, J. Ma, R. Zhang, H. Wang, and Y. Zhang, *IEEE Electron Device Lett.*, **40**, 1399 (2019).
51. J. Yang, S. Ahn, F. Ren, S. J. Pearton, S. Jang, J. Kim, and A. Kuramata, *Appl. Phys. Lett.*, **110**, 192101 (2017).
52. K. Sasaki, "Demonstr. Over 10-A Ga2 O3 schottky barrier diodes fabr. By using high-quality ß- Ga2 O3 3 Homoepitaxial Film." *The 3rd International Workshop on Gallium Oxide and Related Materials* (2019).
53. F. Ren, M. Xaio, P. I. Carey, C. Fares, S. J. Pearton, and M. Tadjer, *SPIE Photonics West 2020*, **11275**, 11280 (2020).
54. W. Li, K. Nomoto, Z. Hu, D. Jena, and H. G. Xing, *Appl. Phys. Express*, **12**, 061007 (2019).
55. W. Li, Z. Hu, K. Nomoto, Z. Zhang, J. Y. Hsu, Q. T. Thieu, K. Sasaki, A. Kuramata, D. Jena, and H. G. Xing, *Appl. Phys. Lett.*, **113**, 202101 (2018).
56. Y. Gao et al., *Nanoscale Res. Lett.*, **14**, 8 (2019).
57. X. Lu, X. Zhang, H. Jiang, X. Zou, K. M. Lau, and G. Wang, *Phys. Status Solidi*, **217**, 1900497 (2019).
58. Q. He et al., *IEEE Electron Device Lett.*, **39**, 556 (2018).
59. S. Jinhyun Noh et al., *Electron Dev. Soc*, **7**, 914 (2019).
60. Z. Galazka, *Semicond. Sci. Technol.*, **33**, 113001 (2018).